AMENDMENT

In the claims:

1 - 3. (Cancelled)

4. (previously presented) A pipeline accelerator, comprising:

a communication bus;

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit; and

wherein each of the hardwired-pipeline circuits is disposed on a respective field-programmable-gate–array die.

5 - 10. (Cancelled)

11. (previously presented) A computing machine, comprising:

a processor;

a pipeline-accelerator configuration registry operable to store hardwired-pipeline-configuration information;

a pipeline accelerator comprising,

a communication bus,

a pipeline-bus interface coupled to the communication bus, and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit disposed on a respective field-programmable-gate–array die; and

a pipeline bus coupled to the processor, the registry, and the pipeline-bus interface of the pipeline accelerator, the pipeline bus operable to carry data between the processor and the pipeline accelerator and to carry the hardwired-pipeline-configuration information from the registry to the pipeline accelerator.

12. (original) The computing machine of clam 11 wherein:

the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus;

the pipeline-bus interface is operable to couple the message to the communication bus;

the pipeline units are each operable to analyze the message;

the identified pipeline unit is operable to accept the message; and

the other pipeline circuits are operable to reject the message.

13. (original) The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

wherein the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus; and

a router coupled to each of the branches and to the pipeline-bus interface and operable to receive the message from the pipeline-bus interface and to provide the message to the identified pipeline unit.

14. (original) The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a secondary bus; and

a router coupled to each of the branches, to the pipeline-bus interface, and to the secondary bus.

15 - 27. (Cancelled)

28. (previously presented) The computing machine of claim 11 wherein the pipeline bus is coupled to the pipeline-accelerator configuration registry via the processor.

29 - 31. (Cancelled)

32. (previously presented) The computing machine of claim 11 wherein at least one of the pipeline units comprises a field-programmable gate array.

33. (previously presented) The computing machine of claim 11 wherein at least one of the pipeline units comprises an application-specific integrated circuit.

34. (previously presented) The computing machine of claim 11 wherein:

at least one of the pipeline units comprises a field-programmable gate array; and

at least one of the pipeline units comprises an application-specific integrated circuit.